OC-3c/OC-12c Asynchronous Transfer Mode (ATM) Load Module

Interfaces

Ixia's ATM Load Module enables high performance testing of routers and broadband aggregation devices such as Broadband Remote Access Server (BRAS) systems and DSLAMs. With full wire-speed IP packet generation and analysis at OC-12 and OC-3 rates, the dual-port ATM Load Module provides a cost-effective, space efficient, multi-port test environment. The ATM Load Module can be optionally configured to support Packet Over SONET (POS); this mode of operation is covered in the OC-3c/OC-12c Packet Over SONET/SDH Load Module data sheet.

The Ixia ATM Load Module supports multiple physical interfaces via modular PHYs, multiple signal rates, and multiple technologies (ATM and POS), providing a very high level of flexibility in a single module. With a RISC CPU per port running Linux, the module provides a powerful platform for running test applications, including IxChariot and Ixia's Routing Protocol Emulation Suites. Combined with a full line of Ethernet, POS, and BERT Load Modules, the ATM Load Module enables Ixia to deliver the industry's most comprehensive test solution.

Specifications

Hot Pluggable Physical Interface	OC-3/OC-12, STM1/STM4
Connector Type	Dual SC with 1310 nm Multi-mode optics or Dual LC using SFP transceiver with 1310 nm multimode or single-mode optics
Signal Rate	OC-3: 155.52 Mbps; OC-12: 622.08 Mbps
Ports Per Load Module	2 ports per module, each may be populated with different physical interface options
Processor/Memory (per port)	1392 MIPS PowerPC/256 Mbytes
Encapsulation	LLC/SNAP per RFC 2684 (1483) VC Multiplexing per RFC 2684 (1483) MPLS LLC per RFC 3035 MPLS Null per RFC 3035
Virtual Circuits	65,536 VC IDs/4,096 VP IDs generated among 4,096 unique streams
Emulation Modes	UNI or NNI per port
ATM Framing	AAL5
Transmit Streams	4,096 among 15 interleaved transmit engines
Transmit Engine	Built-in FPGA logic for wire speed packet generation with timestamps, sequence numbers and packet group signatures. Five User Defined Fields (UDFs) with additional engines for VPI, VCI, IP DA, IP SA, MAC DA, and MAC SA
Receive Engine	Built-in FPGA logic for wire speed packet filtering, capturing, real-time latency for each packet group, data integrity, and sequence checking
Capture Buffer (per port)	8 MBytes
SONET Statistics	Link State, Line Speed, Section LOS, Section LOF, Section BIP (B1), Line AIS, Line RDI, Line REI (FEBE), Line BIP (B2), Path AIS, Path RDI, Path REI (FEBE), Path BIP (B3), Path LOP, Path PLM (C2), Loss of Cell Delineation (LOC)
ATM Transmit Statistics	Cells Sent, AAL5 Bytes Sent, AAL5 Frames Sent, Scheduled Cells Sent, Scheduled Frames Sent, Transmit Throughput, Bits Sent
ATM Receive Statistics	Cells Received, AAL5 Bytes Received, AAL5 Frames Received, AAL5 CRC Errored Frames, AAL5 Length Errored Frames, AAL5 Timeout Errored Frames, Correctable HCS Errors, Uncorrectable HCS Errors, Idle Cells Received, Bits Received
TCP/IP Statistics	IP Packets Received, IP Checksum Errors, UDP Packets Received, UDP Checksum Errors, TCP Packets Received, TCP Checksum Errors

Flexible Packet Generation

Traffic is generated in real-time by intelligent logic implemented in FPGAs on each Ixia port, and frame parameters are user configurable:

- ATM VPI/VCI using 12-bit programmable data generators (UDFs) for VPI, 16-bit for VCI
- Ethernet MAC DA and SA using 48-Bit UDFs
- Five 32-Bit UDFs can be inserted anywhere in the frame
- IP header contents, including incrementing, decrementing, or random IP addresses; IP checksums are generated on the fly in hardware
- Fixed and algorithmic data patterns
- Correct and erroneous IP checksums
- AAL5 frame generation with good or bad CRC

Real–Time Latency

Packets representing different types of traffic profiles can be associated with Packet Group Identifiers (PGIDs). The receiving port measures the minimum, maximum, and average latency in real time, for each packet belonging to different groups. Measurable latencies include Instantaneous Latency, where each packet is associated with one group ID only, and Latency Over Time where multiple PGIDs can be placed in "time buckets" with fixed durations. 64K PGIDs are available per port.

Transmit Scheduler

The packet streams transmit engine can generate multiple streams in sequence, each containing multiple packets with custom characteristics. After all packets in the first stream are transmitted, control is passed to the next defined stream in the sequence. After the last stream in the sequence is reached, transmission may either cease or control may be passed on to any other stream in the sequence. Therefore, multiple streams are cycled through representing different traffic profiles to simulate real world traffic.

Extensive Statistics

Each port accumulates ATM, IP, and SONET statistics in real-time. Both transmit and receive statistics can be viewed on a per-port or per-VC basis. Eight Quality of Service counters are available that enable IP TOS measurements. The user can also define two custom statistics dependent upon source and destination IP addresses, data pattern contents, or error conditions.

Data Capture

A comprehensive set of triggers and filters is available based on VPI/VCI, source and/or destination MAC and/or IP addresses, data pattern, and error conditions. Decodes are available for ICMP, IGMP, IP, TCP, UDP, DHCP, MPLS, OSPF, RIP, ARP, and IPX.

Routing Protocols

The ATM Load Module supports all Ixia Routing Protocol Suites, including BGP-4, OSPF, IS-IS, RIP, LDP, RSVP-TE, PIM-SM, MLD, and IGMP. Protocol emulation operates on a local RISC processor running Linux on each ATM test port. This delivers a highly scalable protocol emulation system that becomes more powerful as ports are added.

Custom Applications

The Linux Software Development Kit (SDK) enables existing Linux applications to be compiled and run on OC-3c/ OC-12c ATM Load Module ports. Additionally, users can develop custom applications which can be integrated into the Ixia test environment.

Product Ordering Information

LM622MR
2-Port ATM/Packet Over SONET Load Module. Supports 622 and 155 Mbps data rates. Configuration options: 1) Requires purchase of 2 PHY modules; 2) Requires purchase of at least 1 operational option – OPTATMMR and/or OPTPOSMR

OPTATMMR
ATM operational option for LM622MR

OPTPOSMR
Packet Over SONET operational option for LM622MR

OC3OC12PHY
Single-port OC-3/OC-12 PHY module for the ATM/Packet Over SONET Load Module. 1310 nm multi-mode optics with dual SC connectors

OC3OC12PHY-SFP
Single-port OC-3/OC-12 PHY module for the ATM/Packet Over SONET Load Module.

SFP-OC12MM1310D
Multi-rate (OC-3, OC-12) SFP transceiver. 1310 nm multi-mode optics with dual LC connectors. Supports diagnostic features

SFP-OC12SM1310D
Multi-rate (OC-3, OC-12) SFP transceiver. 1310 nm single mode optics with dual LC connectors. Supports

diagnostic features